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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Application Number: 09/943,535
Filing Date: August 30, 2001
Appellant(s): CAIRNS ET AL.

Mark D. Saralino
<u>For Appellant</u>

EXAMINER'S ANSWER

This is in response to the appeal brief filed on March 27, 2006 appealing from the Office

action mailed September 01, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related App als and Interfer nc s

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,250,931	Misawa et al	10/05/1993
5,327,254	Daher	07/05/1994
5,390,293	Nishioka et al	02/14/1995
5,767,832	Koyama et al	06/16/1998
6,396,465	Nakagiri	05/28/2002
EP 0,930,716	Gairns et al	7/21/1999

(9) Grounds of Rejection

I.   Claims 1, 2, 5, 9, 10 and 12-14 are rejected under 35 U.S.C. 102(e) as being

anticipated by Nishioka et al(5,390,293).

As to claims 1, 2, 5, 9, 10 and 12-14, Nishioka et al teach a driving arrangement

for an active matrix liquid crystal display comprising: (a) a multi-format digital data

driver arranged to operate in a plurality of different display modes(4096 color

mode(N+M mode) or 512color mode(N mode))(see figures 1, 4, 6 -15, 17 and 19-21;

abstract; column 2, lines 12-47; column 3, lines 1-39; column 4, lines 21-64; column 5,

lines 1-23; column 7, lines 43-51; column 8, lines 29-39; column 9, lines 1-30; column

10, lines 5-47; column 16, lines 1-35; column 17, lines 63-68 and column 18, lines 1-

14), to receive digital input data in a plurality of different color formats(3bits, 60 HZ or 4

bits, 80HZ), and to drive data lines of the liquid crystal display(51) so as to cause an

image to be displayed by the display corresponding to the input data(40-43, 24); and

(b) data analysis means(44) arranged to receive the digital input data(40-43, 24), to

determine the format of the input data, and to control the data driver(44, 48) to operate

in the display mode corresponding to the determined color format of the input data(see

figures 1, 6-15, 19-22; abstract; column 9, lines 1-30; column12, lines 30-67; column

13. lines 3-68 and columns 14-15).   Nishioka et al teach a data driver(44,48)

consuming less power in low resolution display mode(512 or N color mode) compared

to high resolution display mode(4096 or (N+M) color mode)(see figures 1, 4, 6 -15, 17

and 19-21; abstract; column 4, lines 60-64; column 5, lines 13-23; column 8, lines 28-39; column 10, lines 5-47 and column 16, lines 1-10).

As to claim 2, Nishioka et al teach the data analysis means forms part of the data driver(44, 48)(see figure 6).

As to claim 5, Nishioka et al teach the analysis means(44) updating the mode of the data driver at the end of each frame(see figures1, 6-8; column 14, lines 12-68 and column 15, lines 1-9).

As to claim 10, Nishioka et al teach a format control signal(24) having high(4096) and low resolution(512) control signals(see figures 1, 5-7 and column 12, lines 8-12).

As to claim 12, Nishioka et al teach data driver(44, 48) having a plurality of digital data input channels(40-43) arranged to received the digital input data(se figure 6).

As to claim 13, Nishiko et al teach data analysis means(44) having a number of storage registers(60, 62, 66)(see figures 6-7 and column 13, lines 45-63).

II.   Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nashioka et al in view of Daher(5,327,254).

Nashioka fail to disclose a 1-bit overlay mode.

Daher teaches a display device having a on-bit overlay mode(see column 11, lines 52-60 and column 12, lines 1-6).   It would have been obvious to have modified Nashioka et al with the teaching of Daher, so as to efficiently provide a high quality picture.

III.   Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nashioka et al in view of Koyama et al(5,767,832).

Nashioka et al fails to disclose a data driver for providing a lower refresh rate if the input data has remained unchanged.

Koyama et al teach an LCD display driving circuit comprising data driver for outputting a lower refresh rate if the input data has remained unchanged(see figures 1-2; abstract; column 2, lines 3-10 and column 6, lines 53-59). It would have been obvious to have modified Nashioka et al with the teaching of Koyama et al, so as to save power(see abstract and column 1, lines 51-61).

As to claim 8, Koyama teach an LCD display driving circuit having data analysis means having an OR gate(see figure 2 and column 5, lines 5-31).

IV.   Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagiri(6,396,465) in view of Cairns et al(EP 0,930,716).

Nakagiri fails to disclose a variable bit digital to analog converter.

Cairns teach an LCD display driver having a variable bit digital to analog converter(see figures 5, 7, 13-14; column 6, lines 39-58; column 7, lines 1-35 ; column 13, lines 28-58 and column 14, lines 1-8). It would have been obvious to have modified Nakagiri with the teaching of Cairns, so as to provide a more efficient digital to analog converter for performing gamma correction(see column 4, lines 9-39 and column 14, lines 3-8).

V.   Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishioka et al(5,390,293) in view of Misawa et al(5,250,931).

Nishioka et al fail to disclose the thin film transistors of the active matrix arranged in the same substrate.

Misawa et al teach an LCD display having driving means(12, 21) and the thin film

transistors(29) of the active matrix arranged in the same substrate(11)(see figure 1;

abstract and column 4, lines 43-68). It would have been obvious to have modified

Nishioka et al with the teaching of Misawa et al, so as to reduce the number of

connecting wires, ensure more stable connections, minimize space and the number of

parts in providing the display control circuitry.

(10) Response to Argument

Appellants argue that Nishioka et al do not teach input data in plurality of different

color format on page 7. The examiner disagrees with that since Nishioka et al teach

input data(40-43, 24) in plurality of different color format(when the input data(40-43, 24)

is "H" state, it indicated 512 color format; when the input data(24) is "L" state, it

indicated 4096 color format)(see figures 1, 5-7; abstract; column 8, lines 53-68; column

9, lines 1-30; column 11, lines 60-68; column 12, lines 1-14 and lines 54-68; and column

13, lines 1-2).

Appellants argue that Nishioka et al do not teach data analysis means which

determines the color format of the input data and controls the data to operate in different

mode based on the determined color format of the input data on page 7. The examiner

disagrees with that since Nishioka et al teach data analysis means(44, see figures 7-8)

which determines the color format(512 or 4096) of the input data and controls the data

to operate in different mode(512 low color resolution mode or 4096 high color resolution

mode) based on the determined color format of the input data(40-43, 24)(see figures 1,

7-8; abstract; column 8, lines 53-58, column 15, lines 10-39 and rejection paragraph I above).

Appellants argue that Nishioka et al do not teach a driving arrangement controls the data driver to consume less power in low resolution display mode and more power in high resolution display mode based on the determined color format of the input data on page 7. The examiner disagrees with that since Nishioka et al teach a driving arrangement controls the data driver to consume less power in low resolution display mode(512 color mode) and more power in high resolution display mode(4096 color mode) based on the determined color format of the input data(40-43, 24)(see figures 1, 4, 6-8; abstract and column 10, lines 5-47).

Appellants argue that Nishioka et al do not teach a data analysis means for receiving the input data to be displayed and determines the color format of the input data(e.g., whether 1-bit per color, m bits per color, n+m bits per color) on pages 7-8. The examiner disagrees with that since that Nishioka et al teach a data analysis means(44) for determining the color format(4096 or 512) of the input data and controls the data to operate in the display mode(4096(or 4bit), 80HZ mode or 512(or 3bit), 60HZ mode) corresponding to the determined color format of the input data(24) (when the input data(40-43, 24) is "H" state, it indicated 512(3 bits per color) color format; when the input data(24) is "L" state, it indicated 4096(4 bits per color) color format)(see figures 1, 6-8; column 3, lines 29-38; column 8, lines 40-58; column 9, lines 21-25; column 12, lines 56-67; column 13, lines 46-68; column 14 and column 15, lines 1-39).

Appellants state that the FRC ciruit(44) produces 4096 or 512 colors depends on whether the CPU 1 write a "1" or "0" to the FRC circuit 44 on page 10. The examiner disagrees with that since Nishioka et al teach the FRC circuit(44) produces 4096 or 512 colors depends on the input data(24) whether it is "0" or "1"(see figures 1, 5-8; column 12, lines 8-14 and column 15, lines 10-39).

Appellants state that Nishioka et al teaches controlling the particular display mode based on the determination of a user selection on page 10. However, the claim limitations do not required the input data should be automatically generated from a computer. Therefore, Nishiko et al meet all the limitations cited in claims 1, 2, 5, 9, 10 and 12-14(see the rejection and response to the argument above).
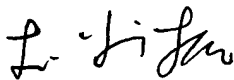
(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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